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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,147	07/16/2003	Robert Ian Gresham	18065	1214

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EXAMINER	
CAVALLARI, DANIEL J	

ART UNIT	PAPER NUMBER
2836	

MAIL DATE	DELIVERY MODE
01/28/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/621,147	GRESHAM, ROBERT IAN	
	Examiner	Art Unit	
	Daniel Cavallari	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-10,12 and 13* is/are pending in the application.

4a) Of the above claim(s) *10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-9,12,13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/29/2007 has been entered.

Response to Arguments

Applicant's arguments with respect to claims 1-5 & 7-9 have been considered but are moot in view of the new ground(s) of rejection.

The Examiner notes claim 10 stands withdrawn and new claims 12 and 13 have been added.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4, 5, 7- 9, & 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi (US 6,054,889)

In regard to Claims 1

- A first circuit portion (Q1e, See Figure 3) corresponding to a first input port, read on by the top port of Rfin1 (See Figure 3).
- A second circuit portion (Q4e) corresponding to a second input port, read on by the bottom port of Rfin1.
- An output port, read on by Output (of 22 and 24).
- Wherein each of the first and second circuit portions includes at least one first transistor, providing a portion of an isolation channel, at least a second transistor,(Q2Ae and Q3Ae of the first and second circuit portions respectively) providing a portion of a transmit channel, and two third transistors (Q5a, Q5b of the first circuit portion and Q6b and Q6a of the second circuit portion) for providing a control bias which selects an input, coupled at its base directly to a base of a corresponding third transistor and to control voltage source (IQ).

In regard to Claim 3

- The third transistors of the first and second portions provides a control bias for selecting which of the first and second input ports are coupled to the output port (See Figure 3).

In regard to Claims 4

- The at least one first transistor (Q1e) comprises two transistors (Q1e and Q1Ae) having emitters coupled to each other and coupled to a collector of the third transistor (26) (See Figure 3).

In regard to Claim 5 & 13

- The switch circuit of claim 1, wherein the at least one second transistor (Q2Ae) comprises three transistors (Q2Ae, Q2e, and Q1Ae, See Figure 3) and the respective emitters of the at least one first transistor and three second transistors are coupled to each other.

In regard to Claim 7

- The switch circuit of claim 1, wherein respective emitters of the at least one first transistor (Q1e) and the at least one second transistor (Q2Ae) are coupled to each other (See Figure 3).

In regard to Claim 8

- The switch circuit of claim 7, wherein the respective emitters of the at least one first transistor (Q1e) and the at least one second transistor (Q2Ae) are additionally coupled to a collector of a respective third transistor (transistors of circuit portion 26, Figure 3).

In regard to Claim 9

A method for providing isolation between at least two inputs at an output comprising the steps of:

- Providing a first (22, Figure 3) channel for each of the at least two inputs including at least one first differential amplifier pair (Q1e, Q1Ae), said first channel providing isolation between the at least two inputs (top and bottom inputs of Rfin1, See Figure 3) and the output of the switch circuit (Output, Figure 3).
- Providing a second channel (24, Figure 3) for each of the at least two inputs including at least one second differential amplifier pair (Q4Ae, Q4e), said second channel providing coupling between one of the at least two inputs and the output of the circuit.
- Providing a control bias (26, 28) which selects one of the at least two inputs and a respective first channel or second channel, said control bias comprising at least one biasing transistor corresponding to a first input port coupled at its base directly to a base of at least one second biasing transistor (Q5a, Q5b) corresponding to a second input port (Q6b, Q6a) (See figure 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 & 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi and Limberg (US 3,798,376).

In regard to Claim 2

Incorporating all arguments above of the switching device taught by Kobayashi, Kobayashi further teaches the use of solid state devices (See Figure 3), but fails to explicitly teach the circuit formed on an integrated circuit.

Limberg teaches solid state components integrated on an integrated circuit (See Column 2, Lines 13-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the switching circuit of Kobayashi into an integrated circuit as taught by Limberg. The motivation would have been the reduced size and weight, increased reliability and economic advantages offered by integrated circuits as opposed to discrete components (See Limberg, column 2, Lines 13-26).

In regard to Claim 12

Kobayashi teaches the at least two third transistors of each of the first and second circuit portions provides a control bias for selecting which of the first and second input ports are coupled to the output port, and the at least one first transistor comprises two transistors (Q1e, Q1Ae) and the at least one second transistor comprises two transistors (Q2Ae, Q2e).

Kobayashi fails to explicitly teach the circuit formed on an integrated circuit.

Limberg teaches solid state components integrated on an integrated circuit (See Column 2, Lines 13-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the switching circuit of Kobayashi into an integrated circuit as taught by Limberg. The motivation would have been the reduced size and weight, increased reliability and economic advantages offered by integrated circuits as opposed to discrete components (See Limberg, column 2, Lines 13-26).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Cavallari whose telephone number is 571-272-8541. The examiner can normally be reached on Monday-Friday 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571)272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Daniel Cavallari

January 18, 2008

1/18/08

MICHAEL SHERRY
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